IN THE CLAIMS

1. (Previously Presented) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the number of semiconductor surface structures includes flash memory cells.

2-9. (Canceled)

10. (Currently Amended) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures and wherein the device includes a synchronous random access memory.

11. (Previously Presented) An integrated circuit, comprising:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the adjacent pair of insulated wordlines, wherein the spacer isolate the buried bitline from the pair of storage node plugs.

12. (Previously Presented) The integrated circuit of claim 11, wherein the bitline plug includes polysilicon.

13. (Previously Presented) The integrated circuit of claim 11, wherein the pair of storage node plugs includes polysilicon.

14. (Previously Presented) The integrated circuit of claim 11, wherein the integrated circuit further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

15. (Previously Presented) The integrated circuit of claim 11, wherein the integrated circuit includes a dynamic random access memory (DRAM).

16. (Previously Presented) The integrated circuit of claim 11, wherein the integrated circuit includes a synchronous random access memory.

17. (Previously Presented) An integrated circuit, comprising:

a central processing unit;

a storage unit, wherein the storage unit comprises:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the pair of adjacent wordlines and isolating the buried bitline from the pair of storage node plugs; and

a system bus for communicatively coupling the central processing unit and the storage unit.

18. (Previously Presented) The integrated circuit of claim 17, wherein the bitline plug includes polysilicon.

19. (Previously Presented) The integrated circuit of claim 17, wherein the pair of storage node plugs includes polysilicon.

20. (Previously Presented) The integrated circuit of claim 17, wherein the storage unit further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

21. (Previously Presented) The integrated circuit of claim 17, wherein the storage unit includes a dynamic random access memory (DRAM).

22. (Previously Presented) The integrated circuit of claim 17, wherein the storage unit includes a synchronous random access memory.

23. (Canceled)

24. (Currently Amended) An integrated circuit device comprising:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug;

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs;

~~The integrated circuit device of claim 23 further comprising~~ a substrate connected to the first and second surface structures, the inner plug, and the pair of outer plugs; and

a pair of outer contact regions, each being connected to one of the outer plugs.

25. (Previously Presented) The integrated circuit device of claim 24, wherein the first and second surface structures are spaced apart along the substrate.

26. (Currently Amended) An integrated circuit device comprising:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug;

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs; and

~~The integrated circuit device of claim 23 further comprising~~ a pair of outer contact regions, each being connected to one of the outer plugs.

27. (Currently Amended) The integrated circuit device of ~~claim 23~~ claim 26, wherein the outer plugs are on opposing sides of the inner plug.

28. (Currently Amended) The integrated circuit device of ~~claim 23~~ claim 26, wherein the pair of spacers are located on opposing sides of the inner plug.

29. (Previously Presented) A integrated circuit comprising:

a processor; and

a storage unit connected to the processor, storage unit including:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer plugs being formed adjacent to and on opposing sides of the inner plug, each one of the outer plugs having upper portions, wherein the upper portions cover top surfaces of the surface structures, wherein the inner plug is beneath the top surfaces of the surface structure; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers.

30. (Previously Presented) The integrated circuit of claim 29 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

31. (Previously Presented) An integrated circuit comprising:

a processor; and

a storage unit connected to the processor, the storage unit including:

first and a second surface structures, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a pair of outer plugs, each having an upper portion covered the top surface of one of the first and second surface structures;

an inner electrical contact connected to the inner plug; and

a pair of spacers for separating the inner plug and the inner electrical contact from the pair of outer plugs.

32. (Previously Presented) The integrated circuit of claim 31 further comprising a pair of outer contact regions, each being connected to one of the outer plugs.

33. (Previously Presented) The integrated circuit of claim 31, wherein the outer plugs are on opposing sides of the inner plug.

34. (Previously Presented) The integrated circuit of claim 31, wherein the pair of spacers are located on opposing sides of the inner plug.

35-40. (Canceled)

41. (Currently Amended) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures ~~The device of claim 6~~, wherein the device further includes a pair of outer contact regions, wherein each of the outer contacts individually couples to one of the outer pair of plugs.

42. (Previously Presented) The device of claim 41, wherein the pair of outer plugs include storage node plugs, and wherein the outer contact regions include storage nodes.

43. (Currently Amended) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures ~~The device of claim 6~~, wherein the number of semiconductor surface structures includes isolated wordlines.

44. (Currently Amended) The device of claim [[6]] 43, wherein the number of plugs include polysilicon plugs.

45. (Currently Amended) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures ~~The device of claim 6~~, wherein the inner plug includes a bitline plug, and wherein the inner electrical contact includes a bitline contact.

46. (Currently Amended) An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures ~~The device of claim 6~~, wherein the device includes a dynamic random access memory (DRAM).

47. (Previously Presented) The device of claim 10, wherein the device further includes a pair of outer contact regions, wherein each of the outer contacts individually couples to one of the outer pair of plugs.

48. (Previously Presented) The device of claim 47, wherein the pair of outer plugs include storage node plugs, and wherein the outer contact regions include storage nodes.

49. (Previously Presented) The device of claim 10, wherein the number of semiconductor surface structures includes isolated wordlines.

50. (Previously Presented) The device of claim 10, wherein the number of plugs include polysilicon plugs.

51. (Previously Presented) The device of claim 10, wherein the inner plug includes a bitline plug, and wherein the inner electrical contact includes a bitline contact.

52. (Previously Presented) The device of claim 10, wherein the device includes a dynamic random access memory (DRAM).